1. A multi-bit split-gate (MSG) flash cell comprising:

a semiconductor substrate having a surface region;

a first drain region and a second drain region formed in said surface region;

a plurality of (N+1) stacked gates separated apart by N select gates (SGs) between said first drain region and said second drain region, where N is any integer;

a first bit line contacting said first drain region;

a second bit line contacting said second drain region; and

a word line contacting said select gate.

2. The MSG flash cell according to claim 1, wherein said surface region is of first conductivity type.

3. The MSG flash cell according to claim 1, wherein said first drain region and second drain region are of second

conductivity type opposite from said first conductivity type.

4. The MSG flash cell according to claim 1, wherein said stacked gates comprise a floating gate and a control gate.

5. The MSG flash cell according to claim 4, wherein said control gate (CG) can be addressed with a different address as a transfer gate (TG).

6. The MSG flash cell according to claim 3, wherein said floating gate comprises a first polysilicon layer separated from said surface region by a first dielectric layer.

7. The MSG flash cell according to claim 3 or 4, wherein said CG and TG comprise a second polysilicon layer separated from said first polysilicon layer by a second dielectric layer.

8. The MSG flash cell according to claim 1, wherein said first bit line and second bit line comprise a third polysilicon layer separated from said first polysilicon layer and second polysilicon layer by a third and a fourth dielectric layer.

9. The MSG flash cell according to claim 1, wherein said word line comprises a fourth polysilicon layer separated from said first polysilicon layer and from second polysilicon layer by said third and said fourth dielectric layers, and from said first and second bit lines by a fifth dielectric layer.

10. The MSG flash cell according to claim 1, wherein said word line comprises a fourth polysilicon layer separated from said third polysilicon layer by a fourth dielectric layer.

11. The MSG flash cell according to claim 1, wherein said select gate is shared by adjacent said stacked gates;

12. The MSG flash cell according to claim 1, wherein the access of said first floating gate transistor is through the turn-on of next adjacent said select gate and next adjacent said floating gate.

13. The MSG flash cell according to claim 1, wherein said word line is oriented generally normal to said first bit line and said second bit line.

14. A method of forming a multi-bit flash cell comprising the steps of:

providing a substrate;

forming a first dielectric layer over said substrate;

forming a first polysilicon layer over said first dielectric layer;

forming a plurality of floating gates comprising said first polysilicon layer, wherein said plurality of floating gates are spaced apart by a plurality of openings over said first dielectric layer;

forming a second dielectric layer over said plurality of floating gates, including said plurality of openings;

forming a second polysilicon layer over said second dielectric layer;

forming a plurality of control gates comprising said second polysilicon layer over said second dielectric layer over said plurality of floating gates;

forming a third dielectric layer over said plurality of control gates;

forming a fourth dielectric layer over the inside walls of said plurality of openings;

forming a third polysilicon layer over first of said plurality of openings to form a first bit line over said substrate, and over last of said plurality of openings to form a second bit line over said substrate;

forming a fifth dielectric layer over said first bit line and over said second bit line; and

forming a fourth polysilicon layer over said fifth dielectric layer, including over said plurality of openings, to form a word line contacting select gates on said semiconductor substrate.

15. The method according to claim 14, wherein said substrate is silicon having active and passive regions.

16. The method according to claim 14, wherein said first dielectric layer is a floating gate oxide having a thickness between about 160 to 180 Å.

17. The method according to claim 14, wherein said first polysilicon layer has a thickness between about 700 to 900 Å.

18. The method according to claim 14, wherein said second dielectric layer is inter-gate oxide having a thickness between about 70 to 80 Å.

19. The method according to claim 14, wherein said second polysilicon layer has a thickness between about 900 to 1100 Å.

20. The method according to claim 14, wherein said third dielectric layer is silicon nitride having a thickness between about 1400 to 1600 Å.

21. The method according to claim 14, wherein said fourth dielectric layer is an oxide spacer comprising a high temperature oxide having a thickness between about 400 to 600 Å.

22. The method according to claim 14, wherein said third polysilicon layer has a thickness between about 1400 to 1600 Å.

23. The method according to claim 14, wherein said fifth dielectric layer is select gate oxide having a thickness between about 150-250 Å.

24. The method according to claim 14, wherein said fourth polysilicon layer has a thickness between about 1400 to 1600 Å.

25. A programming method comprising the steps of:

providing a multi-bit split-gate (MSG) flash cell having a pair of source/drain (S/D) bit lines and N'=(1+N) stacked gates comprising floating gates (FGs) and control gates (CGs) spaced apart with N select gates (SGs) between said bit lines, where N equals any integer;

exchanging the address of control gates with those of transfer gates (TGs);

performing program (write) operation bit by bit, wherein programmed bit is selected by word line, bit line and control gate;

performing erase operation, wherein the erased bits are

selected by word line, bit line and control gate and where the erasing can be bit by bit; and

performing read operation.

26. The programming method according to claim 25, wherein said exchanging the address of CGs with those of TGs is accomplished for CGs of said stacked gates after the first stacked gate.

27. The programming method according to claim 26, wherein said CG of said first stacked gate is impressed with a voltage higher than for said TGs to provide sufficient vertical electric field for programming.

28. The programming method according to claim 25, wherein said TGs between said pair of S/D bit lines are used to turn on the substrate channel below un-selected bits through lower voltage impressed on the TGs.

29. The programming method according to claim 25, wherein said SGs are also used to turn on the substrate channel below SGs during programming.

30. The programming method according to claim 25, wherein said erase operation is page erase operation where erased bits are selected only by word line.

31. The programming method according to claim 25, wherein said programming, erasing and reading an FG transistor is accomplished according to the following table:

Voltage	Write	Erase(1)	Erase(2)	Read
V_{BL1}	5.5	0	0	1.5
V_{CG}	10	0	6u/0s(3)	1.5
V_{SG}	2	13	13	2
V_{TG}	6	--	--	6
V_{BL2}	0.5	0	0	0

(1): Page erase
(2): Page or bit by bit erase
(3): 6V for unselected (u) cell, and 0V for selected (s) cell.